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# Comparative Evaluation of the Loss and Thermal Performance of Advanced Three Level Inverter Topologies

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***Abstract*—This paper presents a comparative evaluation of the loss and thermal performance of two advanced three-level inverter topologies, namely the SiC based T-Type and the Hybrid-NPC, both of which are aimed at reducing the high switching losses associated with a conventional Si based T-Type inverter. The first solution directly replaces the 1200 V primary Si IGBT switches with lower loss 1200 V SiC MOSFETs. The second solution strategically adds 600 V CoolMos FET devices to the conventional Si T-Type inverter to reduce the primary commutation losses. Semiconductor loss models, experimentally verified on calibrated heat sinks, are used to show that both variations can significantly reduce the semiconductor losses compared to the Si based T-Type inverter. The results show that both alternatives are attractive if high efficiencies and reduced thermal stress are major requirements for the converter design.**

***Index Terms*—T-Type, Hybrid-NPC, SiC MOSFET, Si IGBT, CoolMos**

## I. Introduction

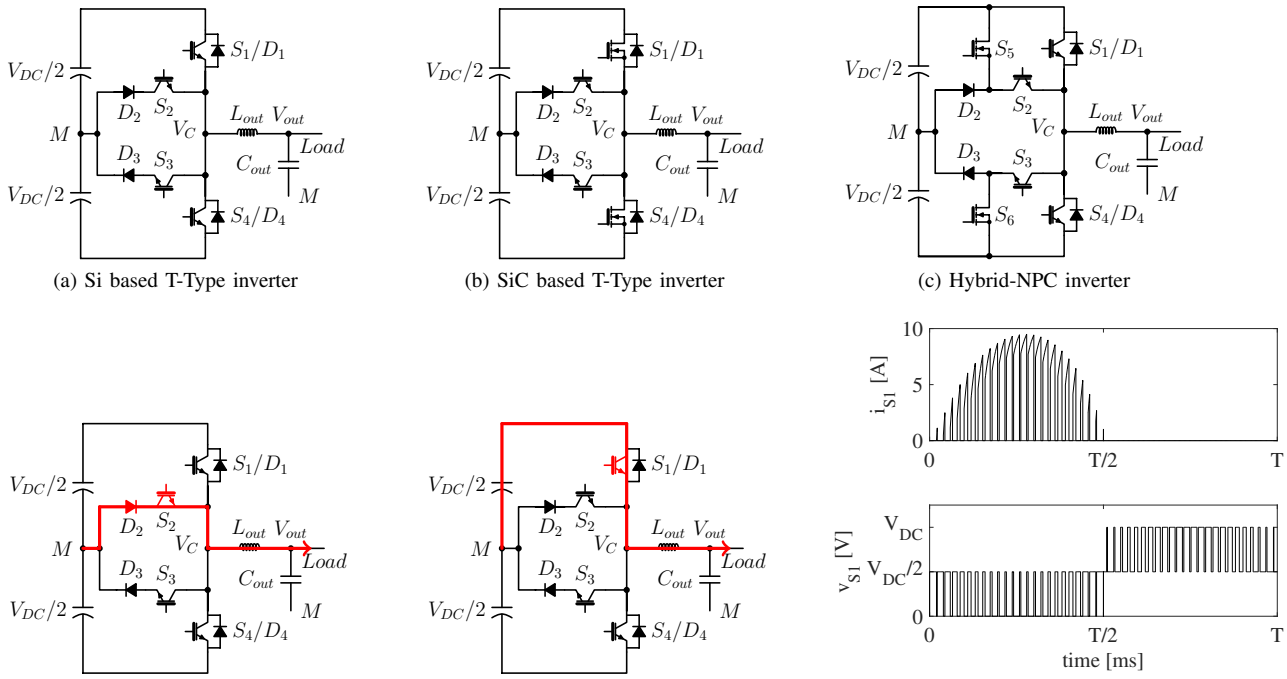
Transformerless photovoltaic (PV) systems are becoming favored in the residential sector due to their reduced size, cost and higher efficiencies compared to transformer based alternatives [1]. To further improve low cost PV systems, previous research has intensively investigated the trade-offs between two- and three-level inverters and has found that three-level inverters have lower total semiconductor losses as the switching frequency increases, and also allow a significant size reduction in the AC filter [2], [3]. Within the three-level inverter alternatives, the Neutral-Point-Clamped (NPC) [4] and the T-Type [5] topologies are widely used, each with particular advantages and drawbacks. For example, since the NPC inverter can use semiconductor devices that need to block only half the DC link voltage, its switching losses are always lower at any given switching frequency compared to the T-Type inverter, whose outer switches must block the whole DC link voltage and hence incur higher switching losses. Nevertheless, the T-Type converter can still achieve lower total semiconductor losses compared to the NPC alternative due to its reduced conduction losses. Hence switching frequency is clearly a crucial parameter in this comparison [3]. Due to recent advances in new semiconductor devices such as silicon carbide (SiC), switching losses in a power converter can be significantly reduced compared to standard Si IGBT alternatives using these devices [6], [7]. However, while the benefits and potential of these devices have been well reported [8]–[12], they are not yet in commonplace usage within commercial converter systems.

A further way to reduce the high switching losses in the T-Type inverter is to strategically add lower voltage switching devices in addition to the conventional T-Type circuit in order to manage the primary commutation events. This approach, called a Hybrid-NPC inverter, has been found to achieve higher efficiencies compared to a conventional T-Type structure with higher voltage (1200 V) Si IGBTs [13]. But to date, only few references are available on this topology alternative [14], [15]. In particular a topological comparative evaluation of the loss and thermal performance between the Hybrid-NPC and the T-Type inverter using next generation switching devices such as SiC under exactly the same operating conditions is not known to the authors. This work therefore presents such a detailed loss comparison for these two advanced inverter alternatives, using semiconductor loss models based on datasheet information (to calculate conduction losses), switching transition measurements (to calculate switching losses) and verification of the loss models thermally on calibrated heat sinks.

## II. T-Type and Hybrid-NPC Inverter

The three inverter alternatives considered in this paper are shown in Fig. 1, with the conventional Si based T-Type structure shown in Fig. 1a as a reference. Its operational principle is illustrated in Fig. 1d-Fig. 1e. Initially, as shown in Fig. 1d, when a zero output voltage is required with a positive output current, diode $D_2$ and switch $S_2$ conduct this load current and the blocking voltage across both $S_1$ and $S_4$ is $V_{DC}/2$.

Then, to achieve a positive output voltage, switch $S_1$ turns on with a commutation voltage of $V_{DC}/2$ and the




(a) Si based T-Type inverter (b) SiC based T-Type inverter (c) Hybrid-NPC inverter

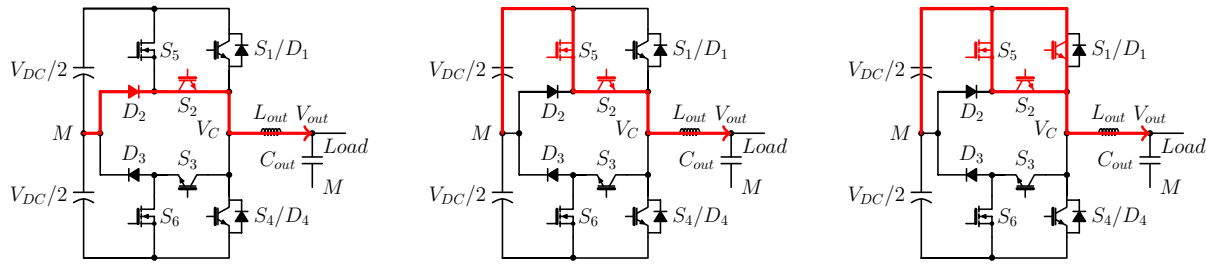
(d) Zero output voltage and positive output current (e) Positive output voltage and positive output current (f) Voltage across and current through $S_1$

Fig. 1. Inverter alternatives used in this study in (a) - (c), commutation from zero output voltage to positive output voltage in (d)-(e) and voltage and current through device $S_1$ in (f)

switching losses associated with this transition. Finally, a zero output voltage is re-established by turning switch $S_1$ off, with associated turn off losses for this transition. This process repeats throughout the positive fundamental half cycle as shown in Fig. 1f. Note that when the converter output voltage is switched to the positive DC rail, switch $S_4$ must block the whole DC link voltage, i.e. $V_{DC}$, which therefore requires $S_4$ to be rated to accommodate the full DC link voltage.

A similar process occurs for the negative fundamental half cycle, with diode $D_3$ and switch $S_3$ conducting current to achieve a zero output stage and switch $S_4$ turning on to achieve a negative converter output stage. Note that when the converter is switching during the negative half cycle, switch $S_1$ must now block the whole DC link voltage, as shown on the right half side of Fig. 1f. Since $S_1$ and $S_4$ need a higher voltage rating to block the whole DC link voltage, in contrast to the inner bi-directional devices $D_2/D_3$ and $S_2/S_3$, which need to block only half the DC link voltage, their switching losses are a major contributor to the overall semiconductor losses. Hence they can be directly replaced with SiC switching devices as shown in Fig. 1b to reduce these switching losses, with the inverter's topological structure and thus its modulation principles unchanged.

Alternatively, additional low voltage rated switching devices $S_5$ and $S_6$ can be added into the circuit, as shown in Fig. 1c, to make a Hybrid-NPC structure. The switching principle of this inverter is a little different as shown in Fig. 2, in that one of either $S_5$ or $S_6$ turn on first to create the positive or negative output voltage as required. Since these devices need only be




(a) Zero output voltage and positive output current (b) Positive output voltage and positive output current (c) Positive output voltage and positive output current

Fig. 2. Operation principle of Hybrid-NPC converter

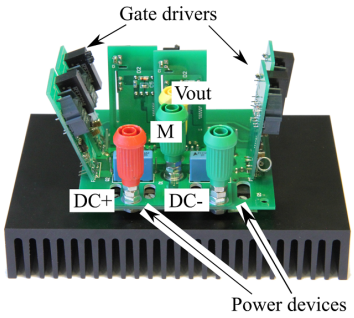
rated to half the DC link voltage, their switching losses will be less than for a conventional T-Type inverter (600 V CoolMos FET devices are used in this work to minimize these switching losses). Once the switching transition is complete, current flows through the two devices $S_5$ and $S_2$ as shown in Fig. 2b (for a positive output voltage and current), which increases their conduction losses to a level similar to a conventional NPC inverter. Switch $S_1$ is then turned on (with almost zero switching losses), and the current flow changes to share between the two conduction paths as shown in Fig. 2c to achieve a similar conduction loss as for a standard T-Type inverter (since the forward voltage drop across $S_1$ is much the same as before).

The turn-off sequence for the Hybrid-NPC is in the reverse order, i.e. $S_1$ first turns off with essentially zero switching losses, and then $S_5$ turns off with appropriate losses against a commutation voltage of $V_{DC}/2$.

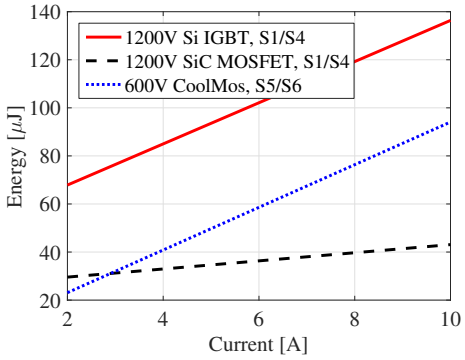
## III. Semiconductor Device Selection

With the operation principles of the three inverter topologies identified, the selection of appropriate semiconductor devices for the topology comparison can now proceed. Since the targeted application for this topology is a grid-connected PV inverter system, the DC link voltage can go up to over 800 V. Thus a 1200 V rated device for $S_1/S_4$ is required. For this voltage range, the usual semiconductor device choice is Si IGBTs, which are known to have higher switching losses than either SiC or CoolMos devices, particularly because of their relatively large turn off energies caused by their long delay tail currents. Fig. 3b and Fig. 3c illustrate this difference, showing the turn on and turn off switching energies for a 1200 V Si IGBT ($S_1/S_4$ in Fig. 1a), a 1200 V SiC MOSFET ($S_1/S_4$ in Fig. 1b) and a 600 V CoolMos ($S_5/S_6$ in Fig. 1c) that were directly measured at appropriate voltages and currents for their T-Type inverter context, using the laboratory prototype shown in Fig. 3a. It can be seen from these results that while the 1200 V Si IGBT turn on energies are not so much larger than the CoolMos device, both the CoolMos FET and the SiC MOSFET show a superior turn off switching loss behavior. This is a particularly interesting observation since the turn off energies have been found to be the limiting factor for high efficient high switching frequency operation of the T-Type inverter [16]. Note also that since PV inverters operate mainly at unity power factor [17], the inner bi-directional device ($S_2/S_3$ in all topologies) switching losses will be essentially negligible and are therefore not included in this switching energy comparison.

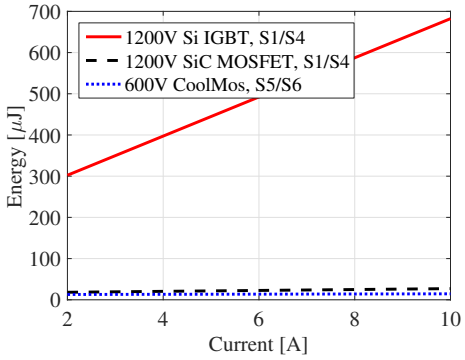
To complete the switching device loss comparison, their forward conduction voltages can be taken from the manufacturer's datasheets. The results are presented in Fig. 4, and show that the SiC MOSFET as a direct replacement to the 1200 V Si IGBT can also greatly reduce conduction losses over the current range of interest. Particularly at low currents, the SiC MOSFET shows a large voltage drop reduction due to its low on-state resistance, while the Si IGBT has a bipolar output characteristic and therefore a more constant and larger voltage




(a) Laboratory prototype




(b) Turn on energies




(c) Turn off energies

Fig. 3. Laboratory prototype and measured switching energies

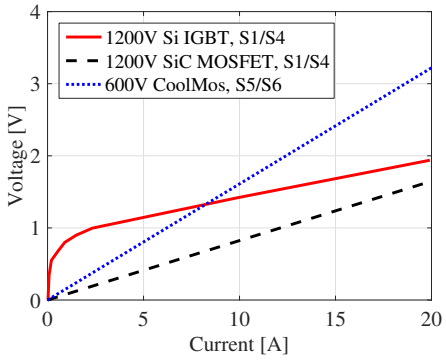



Fig. 4. Forward voltages of the primary devices

drop. Fig. 4 also shows that the 600 V CoolMos device has a relatively large forward voltage compared to the SiC MOSFET due to its Si based semiconductor substrate. Table I lists all semiconductor devices used in this comparison evaluation.

## IV. Loss breakdown analysis

Once the device forward conduction and switching losses have been characterized, a loss breakdown analysis for their operation in the T-Type and Hybrid-NPC converter structures can be conducted. The IGBT conduction loss model is obtained using its dynamic on-resistance $r_{on}$ and zero on-state voltage $V_0$, i.e.

$$P_{con,IGBT} = V_0 I_{AV} + r_{on} I_{rms}^2 \quad , \tag{1}$$

where $I_{AV}$ and $I_{rms}$ are the average and root-mean-square currents through the device. For the SiC MOSFET and the CoolMos FET, only their on resistance $R_{DS(on)}$ is needed to determine conduction losses, i.e.

$$P_{con,FET} = R_{DS(on)} I_{rms}^2 \quad . \tag{2}$$

The conduction losses for the diodes are based on their threshold voltage $V_T$ and dynamic on-resistance $r_{on}$, i.e.

$$P_{con,Diode} = V_T I_{AV} + r_{on} I_{rms}^2 \quad . \tag{3}$$

For the switching energies, Fig. 3b and Fig. 3c show that the switching losses for each device have a linear relationship to the switched current. Therefore, all switching energies can be modeled as a linear equation according to

$$E_{on,S1,4,5,6} = a_{on} i_{out}(t) mod(t) + b_{on} \tag{4}$$

$$E_{off,S1,4,5,6} = a_{off} i_{out}(t) mod(t) + b_{off} \tag{5}$$

where $a_{on}$, $a_{off}$, $b_{on}$ and $b_{off}$ are curve fitting constants for each device derived from the plots shown in Fig. 3. $i_{out}(t)$ is the AC load current and $mod(t)$ is the output voltage modulation function which is defined in the usual way as

$$mod(t) = M sin(\omega t) \tag{6}$$

where M is the modulation index. The overall averaged switching losses can then be calculated as

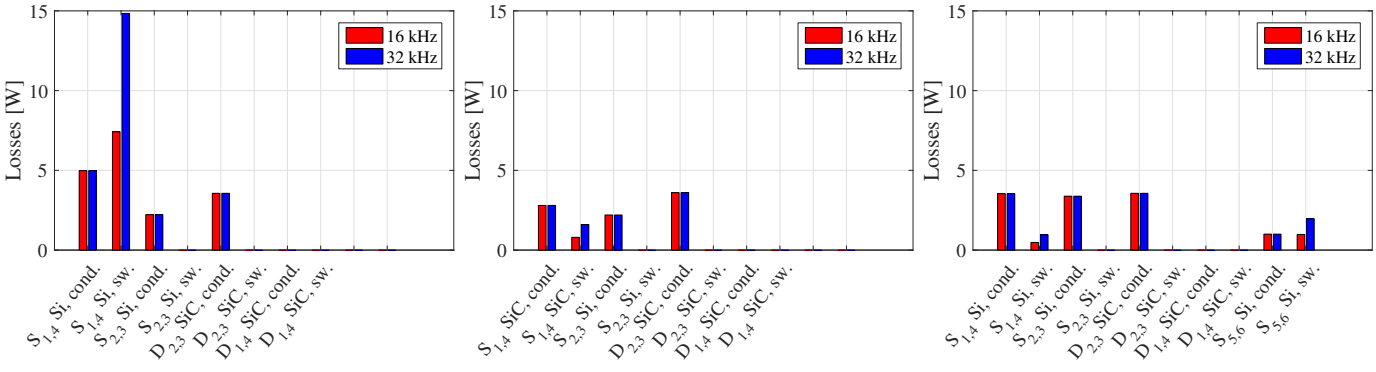
$$P_{sw,S1,4,5,6} = f_{sw} \frac{1}{T} \int_{0+\varphi}^{T/2} (E_{on,S1,4,5,6} + E_{off,S1,4,5,6})\, dt \tag{7}$$

Once these equations are established and the average and rms currents are determined either analytically or via simulations, the total semiconductor losses can be calculated for any given operating point, with an associated device loss breakdown. Fig. 5 shows this loss breakdown for the Si based T-Type, the SiC MOSFET based T-Type and the Hybrid-NPC inverters with the specifications given in Table II, and operating at an output power of 1.5 kW.

From this result, it can immediately be seen that even though the outer switch commutation voltage is only $V_{DC}/2$, switching losses in the 1200 V Si IGBT are the largest loss contributor to the overall semiconductor losses. Obviously, this effect becomes more severe as the switching frequency increases. Both the SiC based T-Type and the Hybrid-NPC substantially reduce these switching losses as shown in Fig. 5b and Fig. 5c. In fact, for this particular example, at a switching frequency of 16 kHz, the switching losses in the 1200 V Si IGBT are 7.4 W while the switching losses in the 1200 V SiC MOSFET are only 0.8 W and the switching losses using the 600 V CoolMos FET device are 1.1 W. Note also that semiconductor losses are more evenly distributed among the devices for these two more advanced arrangements. Thus, both inverter variations are attractive alternatives compared to a conventional T-Type inverter structure when reduced semiconductor losses are an important factor.

TABLE I
Semiconductor devices used

| | Si T-Type | SiC T-Type | Hybrid-NPC |
|---|---|---|---|
| $S_1/S_4$ | IKW15N120T2 | C2M0080120D | IKW15N120T2 |
| $S_2/S_3$ | IKP15N60T | IKP15N60T | IKP15N60T |
| $D_2/D_3$ | C3D10060A | C3D10060A | C3D10060A |
| $S_5/S_6$ | | | SPP20N60S5 |




(a) Si T-Type (b) SiC T-Type (c) Hybrid-NPC

Fig. 5. Loss breakdown analysis for different inverter alternatives. DC link voltage $V_{DC} = 800$ V, filtered output voltage $V_{out,RMS} = 230$ V, output power $P_{out} = 1500$ W

TABLE II
INVERTER SPECIFICATIONS

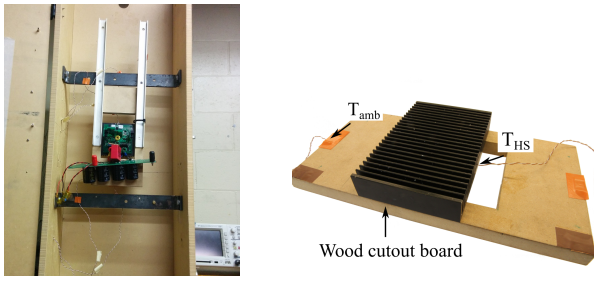
| Symbol | Meaning | Value |
|---|---|---|
| $V_{DC}$ | DC link voltage | 800 V |
| $V_{out}$ | Filtered output voltage, rms | 230 V |
| $f_{out}$ | Fundamental frequency | 50 Hz |
| $L_{out}$ | Filter inductor | 3 mH |
| $C_{out}$ | Filter capacitor | 4.4 µF |
| $M$ | Modulation index | 0.85 |

## V. Loss Model Validation by Thermal Measurements

Since the losses and the loss reduction discussed in this paper relate only to the semiconductor devices, they can be readily validated experimentally. This was done using thermal measurements on the device heat sink since semiconductor device losses lead directly to an increased heat sink temperature. To accurately match these temperature measurements to the semiconductor losses, the converter power stage was located inside an open ended chimney as shown in Fig. 6a. To minimize any thermal influence from the surrounding of the power stage (for instance gate driver circuitry), the heat sink was thermally decoupled from the rest of the power stage circuitry using a wooden panel as shown in Fig. 6b. Then, two temperatures are measured, one at the top of the heat sink $T_{HS}$ and one below the heat sink giving $T_{amb}$, as shown in Fig. 6b. The difference between these readings gives the relative heat sink rise according to

$$\Delta T = T_{HS} - T_{amb} \quad . \tag{8}$$

The measurement was used to carefully calibrate the heat sink using known DC loads. This was achieved by supplying the inverter with a known DC voltage and current (and hence power) with inverter switch states selected such that the semiconductor devices absorb all of the power supplied from the controlled DC source. This is illustrated in Fig. 7 for the switches of the Hybrid-NPC converter, i.e. $S_5$, $S_1$ and $S_4$. Similar results were taken for as many different switch pair combinations as possible (e.g. $S_1$, $S_3$ and $D_3$ as a combination and $D_2$, $S_2$ and $S_4$ as another combination), to achieve a well-defined temperature profile of the heat sink. The injected power corresponds to the thermal energy forced into the heat sink, and is thus responsible for the heat sink temperature rise. Note that several calibration runs are necessary for different power levels to achieve a relation between the injected power and the heat sink temperature rise over a wide range of power loss points, as shown in Fig. 8. The resultant loss profile is linear, as could be expected for a constant heat sink thermal impedance.




(a) Converter placed in chimney

(b) Thermal measurements location

Fig. 6. Thermal measurement setup

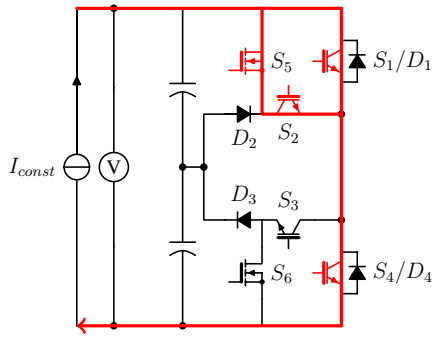



Fig. 7. Switch pair $S_5$, $S_2$, $S_1$ and $S_4$ are conducting

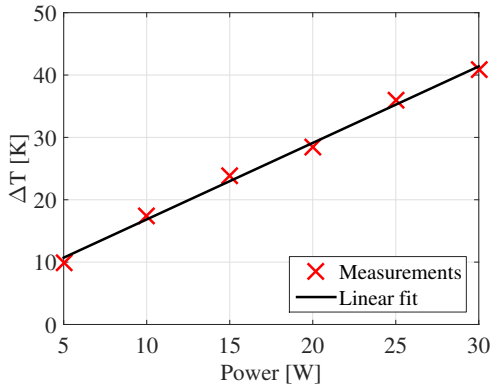



Fig. 8. Device losses versus heat sink temperature rise

## VI. Experimental Results

Once the calibration procedure was completed, the converter was then operated at a number of operating conditions to determine the aggregate semiconductor device losses. Operating the converter using phase disposition (PD) PWM [18], [19] with the parameter specifications provided in Table II, the resulting experimental output waveforms for a 230 V, 50 Hz system at 1.5 kW are shown in Fig. 9. The loss results for different operating conditions such as varying output power and switching frequency are shown in Fig. 10, where the predicted semiconductor losses are compared against the measured semiconductor losses. The results are clearly well within the measurement bounds of the experimental thermal measurement technique, and confirm that both the SiC based T-Type inverter and the Hybrid-NPC inverter achieve a major loss reduction compared to the conventional Si based T-Type inverter. More specifically, at 1.5 kW and 16 kHz, the Si T-Type inverter has total semiconductor losses of 22 W while the SiC based alternative

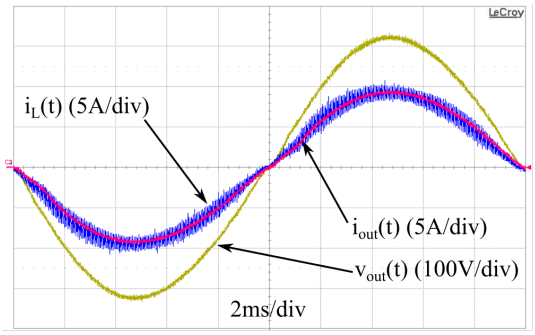
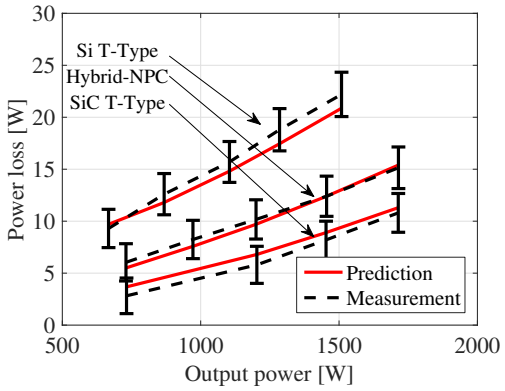
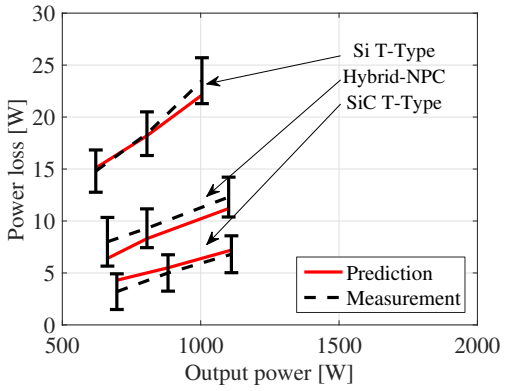



Fig. 9. Experimental output waveforms

has only 9 W losses and the Hybrid-NPC converter shows semiconductor losses of about 13 W. This results in a loss reduction of around 60 % for the SiC based converter and 42 % for the Hybrid-NPC. Hence the Si based T-Type inverter has the highest heat sink temperature rise above ambient at that operating point, shown in Fig. 11, where the heat sink temperature rises for each alternative are presented. In particular, for the conventional T-Type inverter, the temperature rise of the heat sink above ambient is 31.8 °C compared to only 14.6 °C for the SiC alternative and 19.8 °C




(a) Semiconductor losses at 16 kHz




(b) Semiconductor losses at 32 kHz

Fig. 10. Semiconductor losses experimentally obtained via thermal measurements

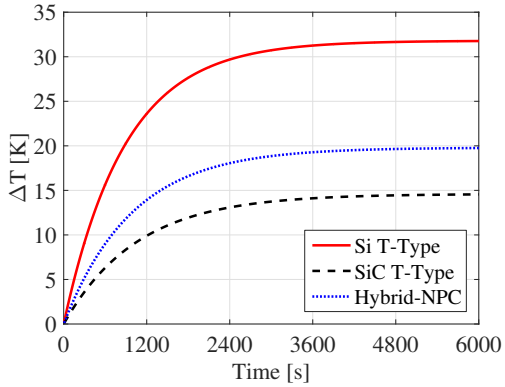



Fig. 11. Heat sink temperature rise of different inverter alternatives

for the Hybrid-NPC. Thus the loss reduction can not only be interpreted in terms of higher efficiency, but there is potential for further cost reduction by using a smaller heat sink.

## VII. Discussion

Two observations from Fig. 10 are worthy of further comment regarding the two converter alternatives. Firstly, while the Hybrid-NPC can substantially reduce its total semiconductor losses compared to the conventional T-Type inverter, its loss reduction is not as good as the SiC based T-Type structure. This can be explained by recognizing that although the switching losses are greatly reduced for the Hybrid-NPC converter, its total semiconductor conduction losses are larger compared to the SiC based T-Type inverter because of the very low on-state resistance of the SiC MOSFETs as shown in Fig. 4. Furthermore, from Fig. 2c, the conduction losses in the inner bi-directional switches $S_2/S_3$ are increased because they conduct current during both the zero converter output period and positive/negative converter output period.

The second observation relates to switching losses. As the switching frequency is increased, the power loss increase is larger for the Hybrid-NPC alternative compared to the SiC based T-Type converter. This can be explained from Fig. 3b, which identifies larger turn on energies for the CoolMos FET relative to the SiC MOSFET. Therefore, at any particular switching frequency, switching losses in the Hybrid-NPC will be higher than the SiC MOSFET based T-Type structure.

## VIII. Conclusion

This paper has compared two promising three-level inverter topologies that aim to reduce switching losses compared to a conventional T-Type inverter structure. The first alternative is to simply replace the lossy 1200 V Si IGBTs with low loss 1200 V SiC MOSFETs. The second alternative strategically adds 600 V CoolMos FET devices to better support the switching transitions. A loss breakdown analysis using a loss model obtained from datasheet information and in-circuit measurement of switching events quantifies the loss reduction for both alternatives. In order to verify these semiconductor

loss models, a simple thermal measurement technique was used based on calibrated heat sinks. The experimentally confirmed results show that a total semiconductor loss reduction of up to 60 % can be achieved using SiC MOSFETs and 42 % for the Hybrid-NPC inverter. Furthermore, this loss reduction for both alternatives has the additional benefit of operating at a significantly lower temperature, which offers further potential for reduced heat sink costs and/or increased inverter life expectancy.

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